CSCI 210: Computer Organization
Lecture 10: Control Flow

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Announcements

- Problem Set 3 Due Friday

- Professor Warford Research Talk, Wednesday

- Professor Beers Thursday

CS History: The If-Else Statement

- Haskell Curry and Willa Wyatt are the first people to describe performing different instructions based on the result of a previous calculation, on the Eniac in 1946
- Early assembly language instructions jumped to a new memory location based on a specific condition, were not general purpose
- Fortran (1957) specifying jumps to three locations at once, depending on whether a calculation was negative, zero, or positive, and gave it the name "if.”
- Flow-matic (Grace Hopper, 1958), used comparisons between numbers and used the name “otherwise” for else
- In 1958, a German computing organization proposed an if statement that took an arbitrary Boolean statement, had an ”else” case, and returned control to immediately after the if/else statement after completing the statement

Logical Operations

- Instructions for bitwise manipulation

Operation	C	Java	MIPS
Shift left	<<	<<	`sll`
Shift right	>>	>>>	`srl`
Bitwise AND	&	&	`and, andi`
Bitwise OR	|	|	`or, ori`
Bitwise NOT	~	~	`nor`

- Useful for extracting and inserting groups of bits in a word

Or Truth Table

	0	***1***
0	0	1
1	1	1

OR Operations

- Useful to set bits in a word
  - Set some bits to 1, leave others unchanged

```
or $t0, $t1, $t2
```

\$t2	0000 0000 0000 0000 0000 1101 1100 0000
\$t1	0000 0000 0000 0000 0011 1100 0000 0000
\$t0	0000 0000 0000 0000 0011 1101 1100 0000

OR Identities (for a single bit)

- x | 0 =
- x | 1 =

01101001 | 11000111

A. 00010000

B. 01000001

C. 10101110

D. 11101111

Nor Truth Table

	0	***1***
0	1	0
1	0	0

NOR Operations

- MIPS has NOR 3-operand instruction
  - a NOR b = NOT (a OR b)

```
nor $t0, $t1, $t2
```

$t2	0000 0000 0000 0000 0000 1101 1100 0000
$t1	0000 0000 0000 0000 0011 1100 0000 0000
$t0	1111 1111 1111 1111 1100 0010 0011 1111

01101001 NOR 11000111

A. 00010000

B. 01000001

C. 10101110

D. 11101111

NOT operations

- Inverts all the bits in a word
  - Change 0 to 1, and 1 to 0

MIPs does not need a NOT instruction because we can use ____ for NOT $t1, $t2

A. NOR $t1, $t2, $zero

B. NOR $t1, $t2, $t3, where all bits in $t3 are set to 1

C. NORI $t1, $t2, 1111111111111111, where NORI is Nor Immediate

D. It does require a NOT operation

E. None of the above are correct

NOR Operations

- MIPS has NOR 3-operand instruction
  - a NOR b == NOT (a OR b)

```
nor $t0, $t1, $zero
```

$t1	0000 0000 0000 0000 0011 1100 0000 0000
$t0	1111 1111 1111 1111 1100 0011 1111 1111

XOR Truth Table

	0	***1***
0	0	1
1	1	0

XOR Operations

- Exclusive OR (written x ⊕ y or x ^ y)
  - Set bits to one only if they are not the same

```
xor $t0, $t1, $t2
```

$t2	0000 0000 0000 0000 0000 1101 1100 0000
$t1	0000 0000 0000 0000 0011 1100 0000 0000
$t0	0000 0000 0000 0000 0011 0001 1100 0000

01101001 XOR 11000111

A. 00010000

B. 01000001

C. 10101110

D. 11101111

XOR Identities (for a single bit)

- x XOR 0 =

- x XOR 1 =

10 & 7

A. 0

B. 2

C. 7

D. 10

E. None of the above

Today: Program control flow

- High level languages have many ways to control the order of execution in a program: if, if-else, for loops, while loops

- Today we will look at how these higher order concepts are built out of MIPS control flow instructions

Control Flow

- Recall the basic instruction cycle
  - IR = Memory[PC]
  - PC = PC + 4

- Both branch and jump instructions change the value of the program counter

Control Flow - Instructions

- Conditional
  - beq, bne: compare two registers and branch depending on the comparison
  - Change the value of the program counter if a condition is true

- Unconditional
  - j, jal, jr: jump to a location
  - Always change the value of the program counter

Control Flow - Labels

- In assembly, we use labels to help us guide control flow. Labels can be the target of branch or jump instructions.
- Example:

```
j Label
…
Label:  add $t1, $t0, $t2
```

- Assemblers are responsible for translating labels into addresses.

C Code

```
if (X == 0)
  X = Y + Z;
```

Assuming X, Y, and Z are integers in registers $t0, $t1, and $t2, respectively, which are the equivalent assembly instructions?

A

```
       beq $t0,$zero, Label
Label: add $t0, $t1, $t2
```

B

```
       beq $t0,$zero, Label
       add $t0, $t1, $t2
Label:
```

C

```
       bne $t0,$zero, Label
       add $t0, $t1, $t2
Label:
```

D – None of these is correct.

If (x < y): Set Less Than

- Set result to 1 if a condition is true
  - Otherwise, set to 0
- `slt rd, rs, rt`
  - if (rs < rt) rd = 1; else rd = 0;
- `slti rt, rs, constant`
  - if (rs < constant) rt = 1; else rt = 0;
- Use in combination with beq, bne

```
slt $t0, $s1, $s2  # if ($s1 < $s2)
bne $t0, $zero, L  #   branch to L
```

Branch Instruction Design

- Why not `blt`, `bge`, etc?
- Hardware for <, ≥, … slower than =, ≠
  - Combining with branch involves more work per instruction
  - `beq` and `bne` are the common case

High level code often has code like this:

```
if (i < j) {
    i = i + 1;
}
```

Assume $t0 holds *i* and $t1 holds *j*. Which of the following is the correct translation of the above code to MIPS assembly (recall $zero is always 0):

```
    slt   $t2, $t0, $t1
    bne   $t2, $zero, x
    addi  $t0, $t0, 1
x:  next instruction
```

A

```
    slt   $t2, $t0, $t1
    bne   $t2, $zero, x
x:  addi  $t0, $t0, 1
    next instruction
```

B

```
    slt   $t2, $t0, $t1
    beq   $t2, $zero, x
    addi  $t0, $t0, 1
x:  next instruction
```

C

D None of the above

```
slt rd, rs, rt
```

if (rs < rt) rd = 1; else rd = 0;

Signed vs. Unsigned

- Signed comparison: `slt`, `slti`

- Unsigned comparison: `sltu`, `sltui`

slt vs sltu

\$s0 = 1111 1111 1111 1111 1111 1111 1111 1111

\$s1 = 0000 0000 0000 0000 0000 0000 0000 0001

	slt \$t0, \$s0, \$s1	**sltu \$t0, \$s0, \$s1**
A	\$t0 = 1	\$t0 = 1
B	\$t0 = 0	\$t0 = 1
C	\$t0 = 0	\$t0 = 0
D	\$t0 = 1	\$t0 = 0

```
slt rd, rs, rt
```

if (rs < rt) rd = 1; else rd = 0;

Questions on BEQ, BNE, SLT?

Reading

- Next lecture: Procedures
  - Section 2.9
- Problem set: Due Friday
- Lab 2: Due Monday